Transient Array Radio Telescope v1.0: Technical Overview

by

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In 1987 Millman and Grabel discarded the historical definition of ‘electronics’ as the science and technology of the motion of charges, preferring instead the operational definition that the primary concern of people doing electronics is information processing. This makes a distinction from energy processing practiced in the rest of electrical engineering. The act of information processing is what gets electronics practitioners involved in the four ‘C’s: communication, computation, control, and components. This practical definition seems to describe well the activities within the Electronics Group in the Physics Department at the University of Otago, and the range of topics covered in this technical report series.

In September 2013, research within the Electronics Group include projects applying inference algorithms to embedded sensors, lightweight GPS tags for birds, modeling and control of a robotic elbow, design and deployment of an underwater glider, analysis of networks of random resistors, electrical impedance imaging, calibration of numerical models for geothermal fields using Bayesian inference, modeling and sampling of Gaussian processes, and efficient algorithms for Markov chain Monte Carlo applied to inverse problems.

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Transient Array Radio Telescope v1.0: Technical Overview

Charles F. Shaw, Timothy C.A. Molteno

Abstract

This document provides an overview of the Transient Array Radio Telescope (TART). An open-source, low-cost radio telescope that operates in the GPS band.

The authors wish to acknowledge the help of the many volunteers who assisted with the refurbishment of the Benmore Radio Observatory facilities, and the kind help of the Helicopter Line who have provided transport of people and material to the telescope site.
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Chapter 1

Overview

The Transient Array Radio Telescope (TART) is a small, low-cost radio telescope that operates in the GPS L1 band. It is designed as platform for the development of new algorithms for radio astronomy. Figure 1.2 shows an overview of the TART.

This report describes the architecture of the TART in its first version. The first version operated with five receivers, each receiver collecting 4ms worth of data digitised at 16 MHz. The sensitivity is therefore limited to bright objects. However the telescope can detect signals from the GPS satellites.

Figure 1.1: The Transient Array Radio Telescope shown with two of eight channels installed. Signals from active GPS patch antennas (1 and 2) are digitised by radio modules (2 and 4). The signal is sent to the base station via CAT-6 cables. The base station comprises the base station board (5), a Startan 3 FPGA development board (6), a RS-232 to USB converter (7), and a Raspberry Pi computer (8). The Pi is connected to a network via Ethernet cable (9). Note that one of the radio modules (2) is shown with RF shielding removed for clarity.
Figure 1.2: The TART consists of up to eight radio modules (4 shown) which are connected to a central base station via Cat-6 cables. Each radio module incorporates a clock conditioner, radio front end, and GPS patch antenna. The base station provides a clock signal (16.368 MHz) and power supply (24 VDC). The incoming data is buffered by the FPGA and transmitted over an RS-232 link to a PC.
Chapter 2

Radio Front-End

Figure 2.1: Photo of the assembled radio module (RF shielding removed for clarity). The board is divided into three areas, each with their own ground plane. The center third of the board is occupied by the power supply and the RS-422 transceivers. The clock conditioner and radio front end are located to the left and right of this respectively. The clock signal track runs along the bottom edge of the board. Status LEDs are provided for Power, Loss of Lock, Lock Detect, and Antenna Flag.

The radio module incorporates a GPS radio front end, a jitter cleaner, power supply, and data transceiver. A photograph is shown in Figure 2.5. This chapter trades the signal from antenna to digitised output of the radio front end. The clock distribution system is discussed in detail in Chapter 3. Chapter 4 discusses the data and power distribution system.
Figure 2.2: Noise factors of components.

Figure 2.3: (a) shows a photograph of the Taoglas A.01.C.301111 two stage 30dB active GPS antenna used for the TART. It has a diameter of 50mm, and is screw mounted and center fed. (b) shows the radiation pattern of the antenna [6]. Section through the XY plane - 0° at top. Note the nearly isotropic radiation pattern above the horizon - ideal for a synoptic wide field radio telescope.
2.1 Antenna

As isotropic antenna allows the entire sky to be viewed at once, but this impacts sensitivity. The response of a hypothetical isotropic antenna would be unaffected by the position of a source.

While an isotropic antenna is unrealisable, some designs come close - particularly those developed for GPS navigation systems. The operating band of the TART allows these antennas to be used. Designing an equivalent antenna from scratch is by no means a trivial exercise.

Corrections for the antennas power reception pattern can be made in the Fourier domain. The output power of an antenna is defined as the convolution it’s Point Spread Function (PSF) with the intensity distribution of the source. This may be undone by applying the convolution theorem. The PSF can be understood as the mirror image of the antennas power reception pattern [8, pg.58].

A photograph of the chosen antenna is shown in Figure 2.3a, and it’s power reception pattern is in Figure 2.3b. This is an active antenna providing 30 dB gain, and incorporates a Surface Acoustic Wave (SAW) filter, and two cascading Low Noise Amplifier (LNA) stages. Out of band rejection is good, and the quoted noise figure is about 3 dB. [6]

Figure 2.4 show an antenna fixed to it’s mount, and deployed on the roof of a the University of Otago Science III building. The heavy concrete base provides stability in all wind conditions, yet easily allows the antennas to be placed in a variety of configurations. It is anticipated that future deployments will use a similar mount.
Figure 2.4: (a) shows a close up of the mounted GPS antenna with the cover removed. This is fixed to the end-cap of a piece of PVC pipe. The pipe is set in 20 kg of concrete in a plastic former. The radio module electronics are housed within the pipe. The CAT-6 cable can be seen entering from the right. In the final implementation the cable will be protected by a system of irrigation pipe. (b) shows an array of these on the roof of physics building.
2.2 Radio Front End

Figure 2.5: The Maxim radio front end IC is provided with a conditioned clock signal and a 2.8v power supply. It down-converts, amplifies, and samples the incoming radio signal. The 2-bit sign/magnitude data is converted to RS-422 levels for transmission to the base station.

The electronics group at the University of Otago has developed systems for wildlife tracking using the Maxim MAX2769B. A desire to capitalize on this expertise has influenced its selection as the radio front end for the TART. Incorporated on the chip is the complete receiver chain, including a dual-input Low Noise Amplifier (LNA) and mixer, followed by the image-rejected filter, Programmable Gain Amplifier (PGA), Voltage Controlled Oscillator (VCO), fractional-N frequency synthesizer, crystal oscillator, and a multi-bit Analogue to Digital Converter (ADC) [2]. The Maxim IC may be configured via a serial interface, or pre-set configurations selected by jumpers. Details of the configuration options selected are presented in Table 2.1.

A schematic of the radio front end and its ancillary components is presented in Figure 2.5. The active antenna (X1) is biased by ANTBIAS (pin 3), and connected to the input of the LNA (LNA2, pin 25) via an AC coupling capacitor (C12). The LNA output (LNAOUT, pin2) is routed externally to the option of an external SAW filter, and in this instance passed via a capacitor (C13) to the mixer input (MIXIN, pin 5).

A 16.368 MHz conditioned clock signal is delivered to pin 15 via a coupling capacitor (C16). This is multiplied (×96) to 1571.328 MHz for low side Local Oscillator (LO) injection into the mixer. The 1575.42 MHz L1 band signal provided to MIXIN is down-converted to 4.092 MHz. It then passes through a 2.5 MHz bandpass filter before amplification by the PGA, and sampling at 16.368 MHz by the ADC.

The sampled 2-bit sign/magnitude signal is finally passed from pins 21 and 22 to the RS-422 transceiver for transmission back to the base station (see Figure A.4).
The power supply is divided into three sections which are isolated by ferrites L3 and L4. To ensure reliability and noise reduction, each of the VCC inputs are bypassed to ground by a capacitor placed as close as possible to the pin. The outputs ANTFLG and LD are connected to LEDs via (internally biased) transistors T1 and T2. These provide a visual indication that the antenna has been detected, and a lock to the clock signal obtained. As the circuits are identical, only LD is shown in the schematic.

The board layout is shown in Figures 2.1 and B.1. The center third of the board is occupied by the power supply and the RS-422 transceivers. The clock conditioner and radio front end are located to the left and right of this respectively.

Isolating the sensitive radio front end from the noise introduced by the various switching components is a key consideration. To this end, a separate ground plane is provided for each section. These are connected at a single point by a 0 Ω resistor. The top and bottom layer ground planes of the power supply are stitched together by vias. The jitter cleaner and radio front end are each provided with RF shields.

Track widths have been maximised where possible to decrease capacitance. This is especially important for the clock line which runs along the bottom of the board. Sharp bends and transitions in track width have been avoided to minimise signal degradation resulting from reflections.

Heat dissipation for the jitter cleaner and radio front end are provided by thermal vias between their ground pad, and the ground plane on the bottom layer. This is particularly necessary for the jitter cleaner which runs very hot.

Table 2.1: The MAX2769B is set to one of its preconfigured states to avoid the complexity of programming through the serial interface. This table shows the details of state 2, set by connecting the PGM and SDATA pins to logic high and SCLK and CS to logic zero [2, pg.17].

<table>
<thead>
<tr>
<th>Reference Frequency (MHz)</th>
<th>Reference Frequency Division Ratio</th>
<th>Main Division Ratio</th>
<th>I &amp; Q or I Only</th>
<th>Number of IQ Bits</th>
<th>I &amp; Q Logic</th>
<th>IF Center Frequency (MHz)</th>
<th>IF Center Bandwidth (MHz)</th>
<th>IF Filter Order</th>
</tr>
</thead>
<tbody>
<tr>
<td>16.368</td>
<td>16</td>
<td>1536</td>
<td>I</td>
<td>2</td>
<td>CMOS</td>
<td>4.092</td>
<td>2.5</td>
<td>5th</td>
</tr>
</tbody>
</table>
Chapter 3

TART Clock Distribution System

An outline of the TART’s clock distribution system is presented in Figure 3.1. The master clock signal for the TART is generated by a Temperature Compensated Crystal Oscillator (TCXO) at the base station, and distributed to eight remote radio modules. It is also supplied to an FPGA, enabling sampling of the incoming data.

The design relies on the use of identical components and equal cable lengths to ensure equal phase delay and coherence between the clock signal provided to each of the radio front ends. A delay locked loop is implemented in the FPGA to synchronise the data.

The RS-422 signal specification implements differential signalling over balanced twisted pairs (see §4.1), and provides a degree of immunity from external interference and cross-talk. Residual jitter is removed by a high performance digital phase locked loop located on the radio module. Schematics for the clock distribution system are presented in Figures A.2 and A.3.

TCXO

The TXC 7Q-16.368MBG fundamental mode TCXO produces a 0.8\text{V}_\text{pp} clipped sine wave output with frequency of 16.368 MHz. It is specifically designed to meet the needs of GPS applications and has excellent frequency stability, in the order of ±0.5ppm [9].

Dual Inverter

A clock signal must be at LVCMOS levels to drive other components in the system. Unfortunately a 16.368 MHz oscillator was unavailable with this output. A dual inverter with Schmitt trigger inputs is utilised to perform the required level shifting. The use of a high speed analogue op-amp or comparator were also valid design options, and seriously considered.

Schmitt triggers are designed with hysteresis in order to provide a level of noise immunity. Because the rising and falling edges of the output are triggered at different thresholds, the duty cycle is slightly uneven. This small variation is tolerated by other components in the system, which trigger only on the rising edge of the clock.
Figure 3.1: A 16.368 MHz clock is supplied to an FPGA, and 8 radio modules (only one is shown). It is generated by a TCXO, and shifted to CMOS levels. The clock is converted to and from a differential signal for transmission over up to 100m of CAT-6 cable. A transceiver attenuates common mode noise. A jitter cleaner then reconstructs a clean clock signal and supplies it to the radio front end.
The input signal is coupled to the dual inverter inputs by a 10 pF capacitor, as shown in Figure A.2. The input is biased set midway between the rails by a voltage divider network. One circuit drives the FPGA, while the second is distributed to eight RS-422 transceivers.

The 0.8 V$_{pp}$ is marginal for driving the inverters. In order to address this issue, a 100 kΩ feed-back resistor is provided between the input and output. When a negative edge on the input drives the output high, the feedback resistor pulls the bias voltage up in preparation for the next positive edge on the input. The converse is true following a negative edge on the input.

**RS-422 Transceiver**

As the clock signal is transmitted over 100 m of CAT-6 cable it is subject to external interference and cross talk. The use of the RS-422 specification for balanced differential transmission allows removal of a large portion of this common mode interference. Transceiver ICs provide the required conversion between LVCMOS to RS-422 signals at each end. Section 4.1 discusses the design rationale in greater detail.

**Jitter Cleaner**

While the RS-422 transceiver is effective in attenuating common mode noise, it is incapable of addressing random jitter. This results from thermal or external noise, and may be modelled as an independent random variable for each conductor. A Silicon Labs Si5317 jitter cleaning clock provides further attenuation of both random and deterministic jitter.

The Si5317 is a propriety digital PLL that incorporates a digital loop filter and Digitally Controlled Oscillator (DCO). The manufacturers of the Si5317 claim a spectacular RMS jitter output of 300 fs [4]. It was chosen principally because it provides a high level of jitter attenuation without clock multiplication.

**Configuration**

The ease with which the Si5317 may be configured is an advantage. The operation frequency, loop bandwidth, reference clock type, and output signal are all set by tri-state jumpers. For the TART all of these except the loop bandwidth are permanently set. The schematic in Figure A.3 provides details of the Si5317’s implementation in the TART.

A frequency range of 16.00 to 17.00 MHz has been chosen by setting FRQSEL[3:0] to HHHM (see Figure A.3). The loop bandwidth may be configured by setting BWSEL[1:0] jumpers in Figure 3.2 according to Table 3.1. A fundamental mode crystal is selected as the reference clock by setting RATE[1:0] to LL. Alternative settings allow the use of a third overtone crystal or an external clock.
The Si5317 has a flexible output driver structure that can drive a variety of loads, including LVPECL, LVDS, CML, and CMOS formats [4]. A CMOS output is selected by setting SFOUT[1:0] LH. The TART uses only one of the Si5317’s two outputs. The second is disabled by a the application of a M to DBL2_BY.

It is possible to adjust the phase of the jitter cleaner output relative to its input. While this feature may be utilised in future designs, in the current implementation both INC and DEC tied to ground.

### Implementation

The Si5317 performs an internal self calibration following a Power On Reset (POR), or the application of a low to RST. The TART uses an RC network to hold RST low for 1 ms after power-up. This helps mitigate the effects of any transients on the power supply. A separate reset signal is considered unnecessary.

Power supply operation, and Loss Of Lock is indicated by the PWR and LOL LEDS shown in Figure 3.2. An output provided for a Loss Of Signal (LOS) alarm is left unconnected because this is also indicated by LLK. Correct operation of the interferometer is not possible in the LLK condition.

The incoming clock signal enters the jitter cleaner ckin+. The RS-232 transceiver output ro_clock is connected via a voltage divider network (R31 & R32), and coupling capacitor (C5) as recommended in the product data sheet [4]. An Epson TSX-3225 38.4 MHz crystal is connected between XA and XB. It has a stability and accuracy of 10 ppm [5].

The jitter cleaner is a digital circuit with a power consumption in the order of 200 mA. Care is required to ensure that it does interfere with the operation of the radio front end, located on the same board. Its power supply is isolated from the main power supply by a ferrite. Each of the VDD inputs are bypassed to ground by a capacitor placed as close as possible to the pin. The jitter cleaner and radio front end are each provided with RF shields.

<table>
<thead>
<tr>
<th>Loop Bandwidth</th>
<th>BWSEL[1:0]</th>
<th>R20</th>
<th>R19</th>
<th>R18</th>
<th>R17</th>
</tr>
</thead>
<tbody>
<tr>
<td>6774 Hz</td>
<td>ML</td>
<td>15k</td>
<td>15k</td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td>1620 Hz</td>
<td>MM</td>
<td>15k</td>
<td>15k</td>
<td>15k</td>
<td>15k</td>
</tr>
<tr>
<td>400 Hz</td>
<td>MH</td>
<td>15k</td>
<td>15k</td>
<td>0</td>
<td>-</td>
</tr>
<tr>
<td>200 Hz</td>
<td>HL</td>
<td>0</td>
<td>-</td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td>99 Hz</td>
<td>HM</td>
<td>0</td>
<td>15k</td>
<td>15k</td>
<td></td>
</tr>
</tbody>
</table>

Table 3.1: The loop bandwidth is set by tri-state jumpers on the BWSEL inputs. This table shows the settings for frequency plan 79 centred on 16.5 MHz, taken from the Si5317 data sheet [4, pg.18].
Figure 3.2: BWSEL1 is set high or low by a single 0 Ω resistor at position R20 or R19. 15 kΩ resistors at both positions select medium. BWSEL0 is set similarly by resistors at R18 and R17. The LLK led warns the jitter cleaner is unable to phase lock to an incoming clock signal. The PWR led indicates operation of the power supply. R11 and R12 are not configurable.
Chapter 4

Data and Power Transmission

Figure 4.1: Photo of the assembled base station, responsible for transmission of data, clock and power to the radio modules. The power supply is at the left, and the connector for the FPGA development board is at the right. A total of eight RJ-45 connectors occupy the top and bottom edges of the board. The clock generator is located at the center.

The TART must record synchronous snapshots of data from eight spatially distributed radio receiver modules. Accordingly, a base station provides the following functionality;

1. Transmission of clock and data signals over extended distances.
2. Distribution of a power supply.
3. A means of interfacing with a computer.

The base station itself comprises three main components (see Fig 4.2):
1. A base station board (The focus of this chapter).
2. A Field Programmable Gate Array (FPGA) (see Chapter 5).
3. A telescope control computer (see Chapter 5).

The first routes the data to the FPGA, and provides a clock signal and power to the radio modules. The second synchronously buffers the data, and transmits it over an RS-232 link. The third schedules the observations and saves the data to a remote network drive.

Clock and data signals are transmitted between each radio module and the base station at RS-422 levels, by three pairs of a CAT-6 cable. The remaining pair transmits 24 VDC.
Figure 4.2: The base station distributes a 24v power supply and 16.368MHz sampling clock to eight GPS radio receiver modules. Incoming data is sampled and written to a remote network drive. This is facilitated by an FPGA and a telescope control computer.
4.1 Data and Clock Transmission

The cables CAT-6 cables are assembled in accordance with EIA/TIA-568A [7], as indicated in Figure 4.3. The non-standard pin and conductor assignments are shown in Table 4.1.

Table 4.1: A CAT-6 EIA/TIA-568A ethernet cable carries power, clock, and data between the base station and each radio module. The (non-standard) assignment of pins and conductors is shown.

<table>
<thead>
<tr>
<th>Pin</th>
<th>Pair</th>
<th>Colour Code</th>
<th>Assignment</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>3</td>
<td>White &amp; Green</td>
<td>Data Magnitude Non-inverting</td>
</tr>
<tr>
<td>2</td>
<td>3</td>
<td>Green</td>
<td>Data Magnitude Inverting</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
<td>White &amp; Orange</td>
<td>Data Sign Inverting</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>Blue</td>
<td>+24v</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>White &amp; Blue</td>
<td>Ground</td>
</tr>
<tr>
<td>6</td>
<td>2</td>
<td>Orange</td>
<td>Data Sign Non-inverting</td>
</tr>
<tr>
<td>7</td>
<td>4</td>
<td>White &amp; Brown</td>
<td>Clock Non-inverting</td>
</tr>
<tr>
<td>8</td>
<td>4</td>
<td>Brown</td>
<td>Clock Inverting</td>
</tr>
</tbody>
</table>

Figure 4.3: An RJ-45 (8P8C) connector and CAT-6 cable assembled in accordance with the EIA/TIA-568A standard for Ethernet cabling. (Public Domain Image).

4.1.1 The RS-422 Transceivers

The clock and data signals are converted from single ended LVCMOS to differential RS-422 by a pair of Linear Technology LTC2851 RS-422 transceivers at either end of the cable. Each transceiver has one input and one output channel.

Each radio module receives a 16.368 MHz clock signal, and transmits 2-bit sign/magnitude data. A second input to the radio module is unused. The differen-
tial inputs are tied to ground, and the corresponding output at the base station left unconnected.

A schematic is shown in Figure A.4 of the RS-422 clock and data transceivers at the base station and radio module. The inverting and non-inverting driver outputs are pins Y and Z respectively. DI is the driver input, and RO is the receiver output. 100Ω termination resistors, match the impedance of the CAT-6 cable, and are provided between the differential pairs to prevent reflections.

A key advantage of the LTC2851 transceivers is their ability to operate from a 3.3V supply. This is a departure from the norm - RS-422 levels are typically ±5 V. Switching noise is controlled by the addition of a 0.1uF capacitor, connected between VCC and ground. Two rows of transceivers can be seen in a photograph of the the bottom side of the base station board (see Figure 4.6b).
4.2 Power Distribution

Power supplies are derived from a 24 V DC system and distributed to each radio over an available twisted pair. The 24 V is stepped down to 5 V using an efficient switching regulator. This is in turn stepped down to 3.3 V by a linear regulator.

Figure 4.4: A 24v supply is provided to the interface board radio modules (via CAT-6 cable). This is stepped down to 5v by a switching voltage regulator and then to 3.3v and 2.8v by a linear regulator. Protection is provided against polarity reversal, high voltage transients, and over-current.
4.2.1 Fault Protection

The TART’s power supply system incorporates a number of layers of fault protection. These include protection against over-current, incorrect voltage and polarity, and voltage transients. Noise control is a particularly important element of the design.

**Fuses** Remote operation of the TART presents servicing challenges. In the event of a failure on one channel, data must be retrievable from the remaining good channels until a repair can be effected. This is facilitated by the protection of each channel with a dedicated fuse.

The power supply of the base station is also protected by a fuse. Unfortunately, an over-current fault here will bring the entire system down. A 500 mA slow blow surface mount fuse is utilised for the base station, and each of the remote stations.

**Incorrect Voltage and Polarity** The OKI-78SR-5 DC/DC converter used accepts an input from 7 to 36 volts, and this provides a certain level of robustness. They can also withstand a sustained short circuit without damage [1].

The DC/DC converter lacks reverse polarity protection. This is provided by the Schottky bridge rectifier (u$11) shown in Figure A.5a. This device also allows safe connection of an AC supply.

**Transient Voltage Spikes** The base station provides two layers of protection against Transient Voltage Spikes as shown in Figure A.5a. A bi-directional Transient Voltage Suppression (TVS) diode (U$12) protects the bridge rectifier, and a uni-directional TVS diode (D4) arrests transients that may develop in the 24 Volt distribution system.

Similarly, a TVS diode (D4) protects the power supply of the remote station against transients in the incoming 24 volt line. This is shown in Figure A.5b.

A measure of protection against transients is also provided by the capacitors C20 an C19 in Figure A.5a and C29 and C30 in Figure A.5b.

**Noise Control** Capacitors are provided between the power rail and ground at various points throughout the power supply to control noise. A common mode choke is provided at the point where the 24 V power supply enters the radio module (see Figure A.5b). This helps to control EMI induced in the extended length of cable between the base station and the radio module.

The Murata Power Solutions OKI-78SR switching regulator is recognised as a potential source of noise, so an EXAR SPX3940 linear regulator (U$13) is chosen for the second stage of voltage regulation (IC18 or U$1 - see Figure A.5).
Figure 4.5: Photo of the radio module’s power supply showing (1) Cable input - 24v (2) Common mode choke (3) Switching DC/DC regulator - 5v (4) Linear regulator - 3.3v. Note that this is a photograph of an early milled prototype board without the distinctive blue solder mask.

4.3 The Base Station Board

The base station board is a two layer 100 × 80 board. It can be easily fabricated in low volume by etching or milling.

The base station board was designed in Cadsoft’s Eagle PCB software. A free version allows board layouts up to 100 × 80, two signal layers, and is supported on multiple platforms. The selection of this software was influenced by a desire to make the TART easily accessible to the open source community.

The power supply is located at the right end of the board. It’s two ground planes on the top and bottom of the board are separated from the board’s main ground plane for noise isolation. A single connection point is provided by a jumper.

The top layer of the board [4.6a] is dedicated to the routing of the 24VDC supply and the clock signal. The clock generator is located at the center of the board. An equal path length is provided for the clock signal between the clock generator at the center of the board and each RS-422 transceiver. This is to minimise phase differences between the clock signal supplied to each radio module.
The bottom layer (Figure 4.6b) routes the clock and data signals between the RJ-45 connectors and transceivers, and also data between the transceivers and FPGA connector at the left of the board.

Photographs of the finished board are shown in Figures 4.1 and 4.6.

Figure 4.6: Photographs of the top (a) and bottom (b) of the hand assembled base station PCB.
Chapter 5

Synchronous Buffering and Data Storage

The Verilog and Python software for buffering, transmission, and the remote storage of data is described in this chapter. The code is implemented on an FPGA, and a Raspberry Pi computer.

The Spartan-3 FPGA board is connected to the radio modules by transceiver interface. It provides a 16.368 MHz clock and eight channels of two-bit sampled radio data, representing the sign and magnitude.

The FPGA samples and buffers the incoming signals before transmitting them over an RS-232 link to the Raspberry Pi. The magnitude bit is currently ignored, and less than eight channels are utilised. Figure 5.1 provides an overview of the functional blocks implemented in Verilog. Sections 5.1 to 5.3 will discuss their operation in detail.

5.1 Delay Locked Loop

Data must be sampled on the negative edge of a clock with matching frequency and phase. This ensures each bit is sampled only once, well away from it’s transition point. Various techniques may be implemented to provide a synchronous sampling clock. A clock signal may be transmitted with the data, or recovered from it using a Delay Locked Loop (DLL).

The TART maximises the data throughput of CAT-6 cable by implementing a DLL for clock recovery. The four conductor pairs available are utilised for power, clock, data sign, and data magnitude. Provision of a return clock signal would have allowed only one channel of data, reducing the sensitivity of the instrument.

The DLL is implemented in the FPGA, and comprises two functional blocks (see Figure 5.2). The first offset_meas measures the phase delay of the input data relative to the clock. The second data_sync applies a phase delay to to ensure the output data is aligned with the clock. Timing diagrams are show in Figures 5.3b and 5.3c respectively.
Figure 5.1: Top level verilog blocks implemented in the FPGA. The DCM multiplies a 50 MHz clock to 160 MHz, and feeds this to the DLL. The DLL uses this to synchronise the incoming data with an externally supplied 16.368 MHz clock. The data is sampled on the negative edge of this clock. The control buffer (activated by RX going high) buffers a snapshot of the incoming data and sends this in blocks to the UART. In the case shown, only four bits per sample are buffered. To avoid RS-232 framing errors, the remaining bits of the byte are set by an LFSR in rand_fill. The sampled data is transmitted down an RS-232 line (RX) to a computer.
Figure 5.2: The DLL aligns the data with the clock to ensure reliable sampling. The offset is first measured, and the data delayed by the appropriate amount. This is done to an accuracy of about \(1/10\) the period - adequate to ensure that the data is not sampled on the rising edge.

5.1.1 Removing Noise Transients from the Data Inputs

Noise transients on the input lines can cause data corruption. These are filtered by the \texttt{wvfm\_avg} module which is implemented within both \texttt{offset\_meas} and \texttt{data\_sync}. The current output state is held until the input has remained stable for three consecutive 160 MHz clock cycles.

The input data level is recorded on the positive edge of the clock, and summed with the previous four values. The output is held low if \(\text{sum} \in \{0, 1, 2\}\), and high if \(\text{sum} \in \{3, 4, 5\}\) (see ??). The phase delay introduced by \texttt{wvfr\_avg} is simply added to the DLL’s input phase delay and eliminated.

5.1.2 Measuring the Offset

The \texttt{offset\_meas} module measures the phase delay of the data relative to the sampling clock. It is supplied with clocks at 16.368 MHz and 160 MHz (\texttt{clk\_samp} & \texttt{clk\_160}, see Figure 5.2). The first matches the frequency of the reference clock used by the radio module. The second (\(\approx 10\times\)) is used for phase measurement, and is generated from a 50 MHz clock by the FPGA’s internal \textit{Digital Clock Manager (DCM)}. Multiplying the sampling clock directly would be preferable, but a minimum input frequency of 18 MHz is required by the DCM [?, pg. 134]. A reset line serves to zero internal counters.

All data channels are assumed to have identical phase delay, because they are transmitted over equal length cables. Therefore only the delay between \texttt{clk\_samp} and
Figure 5.3: The DLL adjusts the phase of the incoming data to match the sampling clock. This is done with sufficient accuracy to ensure the data is sampled well away from its transition. Sampling is on the negative edge of the sampling clock. (a) shows a timing diagram for the DLL. The DLL incorporates offset_meas and data_sync modules. (b) shows a timing diagram for the offset_meas module. This module detects the transition of data_in by averaging over several cycles of clk_160. The phase difference between data_avg and clk_samp is averaged over time, and supplied to the data_sync module. (c) shows a timing diagram for the data_sync module. This module delays data_in by the number of pulses of clk_160 required to ensure that data_out is approximately aligned with the sampling clock.
data_in(0) is measured. This value is fed to the data_sync module by offset(3:0) as a 4-bit integer.

The positive transitions in the sampling clock and data signals are detected on the positive and negative edges of the 160 MHz clock respectively (see ??). A counter (count) is reset on the positive edge of the sampling clock, and is incremented on each positive edge of the 160 MHz clock. The value of count is recorded on the positive edge on data_in(0), and represents the current offset.

The offset is averaged over some time to mitigate any effects of noise. The mode is considered the most suitable measure of central tendency as it’s value is least likely to affected by noise.

The frequency with which each offset value occurs is recorded in a histogram, from which the mode is determined. The offset values are expected to lie in the range 1 → 10, given the 10× relationship between clocks. Sixteen bins, implemented as register histgrm(15:0) are more than sufficient.

The appropriate bin is incremented on the positive data edge, according to the value of the current offset. The value of this bin is then compared to a register (maximum) containing the maximum bin size. If it is larger, the current offset is written to a register (max_bin) representing the current mode. This is in turn output to the data_sync module where it is used to calculate an appropriate delay for the data signals.

The size of register histgrm(15:0) is set to 2^rng_bit, and this determines the maximum value of each bin. Incrementing beyond this would set a bin to zero, and cause the mode to be misreported. As a bin is incremented, it’s value is checked. If it is full, a right bit shift is performed to halve the frequency held in each bin. Blocking assignments within the verilog code allow the increment, check and divide to be executed in one clock cycle. Since every bin is halved, the position of the maximum (and hence the mode) remains unchanged.

### 5.1.3 Aligning the Data with the Sampling Clock

One data_sync module is provided per channel of data, as the functional block diagram in Figure [5.2] shows. Each creates a copy of data_in that is phase delayed by an integer number of 160 MHz clock cycles. The required delay is calculated from the offset(3:0) input.

The counters cnt_hi and cnt_lo are both incremented on the positive edge of the clock, provided data_in has not changed (see Figure ??). If a positive edge edge is detected on data_in, cnt_hi is reset while cnt_lo is incremented. The converse is true on the negative edge.

The always@* block detects when either counter reaches a pre-set value (cnt_val), and sets data_out_next accordingly. When cnt_hi reaches cnt_val, data_out_next is set high. Similarly data_out_next is set low when cnt_lo = cnt_val. The data
output transitions occur on the next positive edge of the clock.

The output data will be in phase with the sampling clock within about 1/10 of the period. The DLL introduces significant phase error (≈ 63 ns) in the data signal, but this does not impact reliability. The data is sampled at the midpoint of each bit, on the negative edge of the sampling clock. Even at maximum phase error there is a safe margin between the data transition and sampling points - see Figure 5.3a.

5.2 The Control Buffer Finite State Machine

![State diagram of the control buffer finite state machine](image)

Figure 5.4: State diagram of the control buffer finite state machine

The control buffer records samples of fixed length from two to eight sources. The sampled data is then sent to the UART for transmission to a PC via an RS232 link. The states of this Finite State Machine (FSM), and the transitions between them are described as follows;

**Idle**: This is the initial state. It is also entered upon system reset, or after all the contents of the memory have been read. Read and Write Pointers are reset to zero. The SAMP_BEG signal selects the write state.

**Write**: In this state, the write pointer is advanced on the positive edge of sample clock. When the memory is full, the FSM changes to the read state.
Figure 5.5: Register transfer level block diagram of the UART module. Note that the receive section is not used at this stage

**Read:** In this state, the contents of the control buffer are written to the UART a block at a time. The read pointer advances on the positive edge of the sampling clock until a **TX_FULL** signal is received from the UART indicating that its FIFO is full. At this point the FSM changes to the read wait state. When the control buffer memory has been fully emptied, the FSM is returned to the idle state.

**Read Wait:** This state is entered from the read state when the UART FIFO is full. When the **TX EMPTY** signal indicates that the UART FIFO has emptied, the FSM returns to the read state.

### 5.2.1 Memory Utilisation and Sample Sizes

The control buffer utilises up to 54 kB of block RAM available on the Xc3s1000 chip. The width of the memory is determined by the number of signals to be simultaneously recorded - between two and eight. The initial implementation used two channels, and the memory was configured as $2 \times 2^{17}$ bits. Eight channels would be configured as $8 \times 2^{15}$ bits. In each case 32 kB of block RAM are used. The use of three or seven channels would be most efficient, and allow the utilisation of 48 kB.

### 5.3 The UART

The Universal Asynchronous Receiver Transmitter (UART) module provides an RS232 interface for communication with a computer. The interface provides adequate speed, is readily available, is straightforward to implement. The required drivers and DB9
connector are available on the Spartan-3 development board used.

The baud rate, number of data bits and stop bits, and the with of the FIFO are defined as parameters. These are set as 115200 kBit/s, 8 bits, 1 bit, and 16 bytes respectively. Existing code for the UART [1] has been modified to suit this application.

The UART module incorporates a baud rate generator, a receive unit, a transmit unit, and two FIFOs. While the facility for full duplex communication is provided, only the transmit functionality is used a this time.

Each word transmitted contains a one bit sample from up to eight input channels, or a two bit sample from up to four channels. This is dictated by the maximum word size in the RS232 standard. Implementing a second RS-232 port would allow eight two bit channels to be transmitted. This could be extended further by sending multiple bytes sample.

At various stages of the TART’s development, only two, three, or four channels have been used. The remaining bits are set by the **rand_fill** module to prevent framing errors (see §5.3.1). At present six one-bit channels are used. In this case the **rand_fill** module is not required, and the unused bits are simply set to zero.

### 5.3.1 Prevention of Framing Errors

In RS-232 communication, an eight bit byte is typically framed by a low start bit, and a high stop bit. For example the ASCII code for zero is transmitted as \(0001100001\) including the start and stop bits (shown bold).

Suppose a continuous stream of these zeros is transmitted. If synchronisation was lost, the same data stream could be misinterpreted as the ASCII character commonly used for XON \((11_{16})\).

\[
\begin{array}{cccccccc}
0 & 0011 & 0001 & 10001 & 10000 & 010001 & 10001 & 10001
\end{array}
\]

In normal circumstances transmission of a continuous stream of identical characters is rare, and framing errors are recovered from quickly. Where transmission of a repeating sequence is likely, precautions should be taken to prevent framing errors.

During early testing, only two of the eight available channels were used. The first six bits of each recorded byte were therefore zero. A value of \(48_{10}\) was added so the data was transmitted as ASCII \(\{0, 1, 2\}\). This allowed the incoming data to be displayed in a terminal window in a human readable format.

The **rand_fill** module (see ??) was introduced to prevent framing error described above. This module utilised a Linear Feedback Shift Register (LFSR) to generate the
first six digits. An LFSR can generate a maximal length pseudo-random sequence of period \(2^n - 1\) - 63 in this case. This strategy eliminated long repeated runs, proved effective in the prevention of framing errors.

5.4 Data Collection and Management.

The data transmitted by the radio modules must be collected and stored for later analysis. This is facilitated by a Spartan-3 FPGA development board and a Raspberry Pi computer. The latter executes Python code to encapsulate the data and save it to a remote network drive.

5.4.1 Recording an Observation

The process of data sampling and storage is initiated at regular intervals by a cron job which executes a shell script. The script in turn executes the `sig_acquire.py` (see ??). The functionality of this python code is outlined below:

1. Reads command line arguments and configuration file.
2. Performs necessary co-ordinate transformations.
4. Opens and configures the RS-232 port.
5. Generates an accurate UTC time stamp using NTP.
6. Initiates data sampling on the FPGA.
7. Reads data from RS-232 port as a string.
8. Converts the string to an integer array.
9. Creates an `observation` object from integer array and configuration data.
10. Saves the `observation` object to a (cpickle) file.

The structure of the observation object is shown in Figure 5.6.

Required Preparation. For observations to be recorded a cron job must be set up, a shell script prepared, and the serial port opened. The crontab file is edited by issuing the command `crontab -e`

```bash
# minute hour day_of_month month day_of_week command
*/1 * * * * cd /homecharles/projects/TART/software/tools/operation;sh acquire$
```

The following shell script runs `sig_acquire.py`. It is automatically executed by a cron job at one minute intervals.

```bash
#!/bin/sh
TART=/home/projects/TART/software/operation
/usr/bin/python $(TART)/sig_acquire.py --config-file $(TART)/telescope_config.json --data-directory /freenas/telescope/data/
```
Figure 5.6: The sampled data is stored as a vector of 8-bit integers. Each bit represents a 1-bit sample from a particular channel. When less than 8 channels are connected, \textit{num\_ant} allows invalid data to be ignored. The position of antennas and time of observation is also recorded. This information may be recorded the \textit{save} method. A vector of bi-polar binary data for a given channel may recovered be \textit{get\_antenna} method. Recovering data on demand reduces file size considerably.

The required serial port is open and set using the \texttt{stty} command:

\begin{verbatim}
stty -F /dev/ttyUSB0 115200 ~cstopb
\end{verbatim}

In the example a USB RS-232 device is opened. The baud rate and the number of stop bits are set to 115200 and one respectively.
Chapter 6

Results

This chapter details some of the early observations made with the first version of TART.

6.1 Callibration

6.2 Siderial Motion

6.3 Visibilities

6.4 Antenna Characterization

The GPS satellites provide ideal “test stars” for the TART. Their position and signal strength is well characterized. We can therefore use them to calibrate the radiation patterns of the TART antennas.

The procedure is straightforward. Each observation is split into its separate antenna signals, and the signals are converted to baseband, corrected for doppler shift, and correlated with the PRN codes from the 31 GPS satellites.

The height of the maximum correlation peak is used as a measure of signal strength. The azimuth and elevation of each satellite are calculated from ephemeris data, and a healpix map of the sky is updated with the signal strength.

Figure ?? shows the resulting measurement of a GPS patch antenna radiation pattern. It is immediately clear that these patterns are complex, showing large changes with relatively small changes in satellite position.

We can conclude from this that a simpler antenna – perhaps a simple folded monopole – might exhibit a less complex response, and make imaging easier.
Appendix A

Schematics

Figure A.1: Schematic of the radio front end.
Figure A.2: Schematic of the clock generator. TCXO provides $0.8V_{pp}$ biased at mid rail by ac coupling capacitor and voltage divider. Inverter level shifts to LVCMOS voltages. Feedback resistor is necessary to ensure a fast output slew rate given the low input signal levels. CLK_OUT is passed to an RS-232 transceiver.

Figure A.3: Schematic of the Jitter Cleaner.
Figure A.4: Schematics of the base station and radio module transceivers, (a) and (b) respectively.
Figure A.5: Power supply schematics for the base station (a), and the radio module (b).
Figure B.1: The radio module is a two layer $100 \times 50$mm board. The top and bottom layers are shown in (a) and (b) respectively. Note the division of the board into sections, and the separation of ground planes. Top and bottom layer ground planes for the power supply are stitched together. All components are placed on the top layer of the board to facilitate the use of a reflow oven.
Figure B.2: Top (a) and bottom (b) layers of the base station board - dimensions $100 \times 80\text{mm}$.
References


[9] TXC corporation. *SMD Temperature Compensated Crystal Oscillators 3.2 by 2.5 by 1.0 mm Q Series*. 